SAR WITH PARTIAL CAPACITOR SAMPLING TO REDUCE PARASITIC CAPACITANCE

ABSTRACT OF THE DISCLOSURE

SAR with partial capacitor sampling to reduce parasitic capacitance. An analog-to-digital convertor is disclosed with reduced parasitic capacitance on the input during a sampling operation. A charge-redistribution, binary-weighted switched-capacitor array is included having a plurality of array capacitors that each have a commonly connected plate interfaced to a first common node and a switched plate, the switched plate operable to be switched between first and second reference voltages during a redistribution phase and select ones of the capacitors additionally operable to be switched to the input during a sampling phase. Each of the array capacitors has a parasitic capacitance associated therewith. A compensation capacitor having a common plate is connected to the first common node and a switched plate, the compensation capacitor operable to be switched to the input during the sampling phase and to the first reference voltage during the redistribution phase. The compensation capacitor has a parasitic capacitance less than the parasitic capacitance of the combination of all of the non select ones of the array capacitors. A comparator compares the voltage on the first common node to a compare reference voltage during the redistribution phase. A successive approximation controller is provided for switching the switched plate of the array capacitors between the first and second reference voltages in accordance with a successive approximation algorithm during the redistribution phase.